METHOD AND STRUCTURE TO FORM CAPACITOR IN COPPER DAMASCENE PROCESS FOR INTEGRATED CIRUCIT DEVICES

ABSTRACT OF THE DISCLOSURE

A method and resulting structure of forming a metal on metal capacitor structure for an integrated circuit device, e.g., mixed signal. The method includes forming a dual damascene structure, where the structure has a first conductive portion comprising copper material that is separated by a dielectric material from a second conductive portion. The second conductive portion is coupled to the first conductive portion underlying the dielectric material through a third conductive portion. The first conductive portion, the dielectric material, and the second conductive portion form a substantially planar surface region opposing the third conductive portion. The first conductive portion and the second conductive portion is coupled through the third conductive portion define a first electrode. The method selectively removing the dielectric material between the first conductive portion and the second conductive portion to form an opening defined by the first conductive portion and the second conductive portion. The method forms an insulting layer within with opening to define a capacitor dielectric layer therefrom. The method also forms a copper layer overlying the insulating layer to a height above the substantially planar surface to form a second electrode. The method also planarizes the copper layer to define the second electrode.

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